WHAT IS CLAIMED IS:

1. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side, a second side and a thickness;

forming a plurality of polymer filled trenches on the first side between the dice having a depth less than the thickness;

thinning the substrate from the second side to expose the polymer filled trenches; and

forming a plurality of grooves through the polymer filled trenches to singulate the dice.

2. The method of claim 1 wherein the polymer filled trenches have a first width and the grooves have a second width less than the first width.

3. The method of claim 1 further comprising forming a first polymer layer on the first side prior to the thinning step and a second polymer layer on the second side after the thinning step.

4. The method of claim 1 wherein the forming the plurality of polymer filled trenches step is performed by scribing the substrate and filling the trenches with a polymer material.

5. The method of claim 1 wherein the thinning the substrate step is performed by planarizing the substrate.

6. The method of claim 1 wherein the thinning the substrate step is performed by planarizing and then etching the substrate.

7. The method of claim 1 wherein the thinning the substrate step is performed by etching the substrate.

8. The method of claim 1 wherein the forming the grooves step is performed by sawing through the polymer filled trenches.

9. The method of claim 1 wherein the substrate comprises a semiconductor wafer, the first side comprises a circuit side of the wafer and the second side comprises a back side of the wafer.

10. The method of claim 1 further comprising forming a plurality of conductive vias in the dice.

11. The method of claim 1 further comprising forming a plurality of conductive vias in the dice comprising conductive members, and etching the substrate to expose portions of the conductive members to form a plurality of pins.

12. The method of claim 11 further comprising depositing a non-oxidizing layer on the portions of the conductive members.

13. The method of claim 1 further comprising forming a plurality of conductive vias in the dice comprising conductive members, etching the substrate to expose tip portions of the conductive members, and forming a plurality of conductive members on the second side in electrical communication with the tip portions.

14. The method of claim 1 wherein the substrate comprises a first conductivity type and a portion with a second conductivity type and further comprising forming a conductive via in the substrate and in the second portion.

15. The method of claim 1 further comprising following the thinning step etching the substrate to a second thickness of about 3$\mu$m to 250$\mu$m.

16. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a semiconductor substrate having a circuit side and a back side;

forming a plurality of trenches part way through the substrate located proximate to peripheral edges of the dice;

depositing a polymer material in the trenches;

thinning the substrate from the back side to contact the polymer material in the trenches; and

singulating the dice by forming grooves through the trenches and the polymer material.

17. The method of claim 16 further comprising forming a circuit side polymer layer on the circuit side prior to the singulating step.

18. The method of claim 16 further comprising forming a back side polymer layer on the back side following the thinning step.

19. The method of claim 16 wherein the thinning step is performed by mechanical planarization of the substrate.

20. The method of claim 16 wherein the thinning step is performed by mechanical planarization followed by etching of the substrate.

21. The method of claim 16 wherein the thinning step is performed by chemical mechanical planarization of the substrate.

22. The method of claim 16 wherein the thinning step is performed by etching the substrate.

23. The method of claim 16 wherein the forming the plurality of trenches step is performed by scribing the substrate.

24. The method of claim 16 wherein the forming the plurality of trenches step is performed by etching or lasering the substrate.

25. The method of claim 16 further comprising prior to the singulating step testing the components on the substrate.

26. The method of claim 16 further comprising providing the dice with a plurality of die contacts, forming a plurality of conductive vias in the dice in electrical communication with the die contacts, and forming a plurality of terminal contacts on the back side in electrical communication with the die contacts.

27. The method of claim 16 further comprising providing the dice with a plurality of die contacts, forming a plurality of conductive vias in the dice in electrical communication with the die contacts, and forming a plurality

of terminal contacts on the circuit side in electrical communication with the die contacts.

28. The method of claim 16 further comprising providing the dice with a plurality of die contacts, forming a plurality of conductive vias in the dice in electrical communication with the die contacts, and forming a plurality of terminal contacts on the circuit side and on the back side in electrical communication with the die contacts.

29. The method of claim 16 further comprising forming a plurality of conductive vias in the dice comprising conductive members, and etching the substrate to expose portions of the conductive members to form a plurality of pins.

30. The method of claim 29 further comprising depositing a non-oxidizing layer on the portions of the conductive members.

31. The method of claim 16 further comprising forming a plurality of conductive vias in the dice comprising conductive members, etching the substrate to expose tip portions of the conductive members, and forming a plurality of conductive members on the second side in electrical communication with the tip portions.

32. The method of claim 16 wherein the substrate comprises a first conductivity type and a portion with a second conductivity type and further comprising forming a conductive via in the substrate and in the second portion.

33. The method of claim 16 further comprising following the thinning step etching the substrate to a thickness of about 3$\mu$m to 250$\mu$m.

34. A method for fabricating semiconductor components comprising:

providing a semiconductor substrate comprising a plurality of semiconductor dice, the substrate having a first side, a second side and a thickness;

forming a plurality of trenches on the first side in a pattern along peripheral edges of the dice, each trench having a depth less than the thickness;

forming a first polymer layer on the first side and in the trenches to form polymer filled trenches;

thinning the substrate from the second side to expose the polymer filled trenches;

forming a second polymer layer on the second side; and

singulating the dice through the polymer filled trenches such that each component includes a semiconductor die covered on six surfaces by a portion of the first polymer layer, a portion of the second polymer layer, and portions of the polymer filled trenches.

35. The method of claim 34 wherein the substrate comprises a semiconductor wafer having streets separating the dice, and the trenches are formed in the streets.

36. The method of claim 34 further comprising forming a plurality of terminal contacts on the first polymer layer in electrical communication with the dice.

37. The method of claim 34 further comprising forming contact bumps on the dice prior to forming the first polymer

layer, forming the first polymer layer on the contact bumps, and then forming terminal contacts on the contact bumps.

38. The method of claim 34 wherein the forming the first polymer layer step comprises forming a dam on the first side enclosing an area on the substrate, and depositing a polymer material on the area within the dam.

39. The method of claim 34 wherein the forming the first polymer layer step comprises molding, stenciling or screen printing.

40. The method of claim 34 wherein the thinning step is performed by depositing a support dam on portions of the substrate and then planarizing the substrate.

41. The method of claim 34 wherein the thinning step is performed by wet etching, dry etching or plasma etching the substrate.

42. The method of claim 34 wherein the thinning step is performed by chemically mechanically planarizing the substrate.

43. The method of claim 34 wherein the thinning step is performed by mechanically planarizing then etching the substrate.

44. The method of claim 34 further comprising providing the dice with a plurality of die contacts, forming a plurality of conductive vias in the dice in electrical communication with the die contacts, and forming a plurality of terminal contacts on the second side in electrical communication with the die contacts.

45. The method of claim 34 further comprising providing the dice with a plurality of die contacts, forming a plurality of conductive vias in the dice in electrical communication with the die contacts, and forming a plurality of terminal contacts on the first side in electrical communication with the die contacts.

46. The method of claim 34 further comprising providing the dice with a plurality of die contacts, forming a plurality of conductive vias in the dice in electrical communication with the die contacts, and forming a plurality of terminal contacts on the first side and on the second side in electrical communication with the die contacts.

47. The method of claim 34 further comprising providing the dice with a plurality of die contacts, forming a plurality of conductive vias in the dice in electrical communication with the die contacts, forming a plurality of conductors on the second side in electrical communication with the conductive vias, and forming a plurality of terminal contacts on the second side in electrical communication with the conductors.

48. The method of claim 47 wherein the terminal contacts are offset with respect to the die contacts.

49. The method of claim 34 further comprising providing the dice with a plurality of die contacts, forming a plurality of conductive vias in the dice comprising conductive members in electrical communication with the die contacts, and etching the substrate to expose at least a portion of each conductive member.

50. The method of claim 34 further comprising providing the dice with a plurality of die contacts, forming a plurality of conductive vias in the dice comprising conductive members in electrical communication with the die contacts, and etching the substrate to expose portions of the conductive members, forming a plurality of conductors on the second side in electrical communication with the conductive members.

51. The method of claim 34 further comprising forming a plurality of terminal contacts on the second side in electrical communication with the conductive members comprising ball or bumps in a grid array.

52. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side, a second side and a thickness;

forming a plurality trenches between the dice, each trench having a first width and a depth less than the thickness;

depositing a polymer material into trenches;

thinning the substrate from the second side to expose the polymer material;

testing the dice on the substrate; and

forming a plurality of grooves through the polymer material and the substrate to singulate the dice, each groove having a second width less than the first width.

53. The method of claim 52 wherein each component comprises a semiconductor die having a circuit side, a back side, and four edges covered by portions of the polymer material.

54. The method of claim 52 wherein the thinning step comprises mechanical planarization.

55. The method of claim 52 wherein the thinning step comprises mechanical planarization followed by etching to remove grind damage.

56. The method of claim 52 wherein the thinning step comprises etching the substrate from the second side.

57. The method of claim 52 wherein the thinning step comprises etching the substrate from the second side.

58. The method of claim 52 wherein the thinning step comprises etching the substrate from the second side to a second thickness of 57 about 10 $\mu$m to 250 $\mu$m.

59. The method of claim 52 further comprising forming a plurality of terminal contacts on the circuit side in electrical communication with the dice.

60. The method of claim 52 further comprising forming a plurality of contact bumps on the dice, and then forming a plurality of terminal contacts on the contact bumps.

61. The method of claim 52 wherein the first side comprises a circuit side of a wafer containing a plurality of integrated circuits.

62. The method of claim 52 wherein the second side comprises a back side of the wafer.

63. The method of claim 52 further comprising forming a first polymer layer on the first side and a second polymer

layer on the second side prior to the forming the grooves step.

64. The method of claim 52 wherein the forming the plurality of trenches step is performed by scribing the substrate.

65. The method of claim 52 wherein the forming the plurality of trenches step is performed by etching the substrate.

66. The method of claim 52 wherein the testing the substrate step comprises burn-in testing.

67. The method of claim 52 wherein the forming the first polymer layer step comprises forming a dam on the first side enclosing an area on the substrate, and depositing a curable polymer on the area within the dam.

68. The method of claim 52 wherein the forming the first polymer layer step comprises molding, printing or stenciling a polymer material.

69. The method of claim 52 wherein the first polymer layer comprises a resist or a photopolymer.

70. The method of claim 52 further comprising forming a plurality of conductive vias in the dice and a plurality of terminal contacts on the second side in electrical communication with the conductive vias.

71. The method of claim 52 further comprising forming a plurality of conductive vias in the dice and a plurality of

terminal contacts on the first side in electrical communication with the conductive vias.

72. The method of claim 52 further comprising forming a plurality of conductive vias in the dice and a plurality of terminal contacts on the first side and on the second side in electrical communication with the conductive vias.

73. The method of claim 72 wherein the terminal contacts on the second side are offset with respect to the conductive vias.

74. The method of claim 52 wherein the second polymer layer comprises a polymer material that is opaque to radiation at a selected wavelength.

75. The method of claim 52 wherein the second polymer layer comprises a photo polymer.

76. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side, a second side and a thickness, the dice comprising a plurality of die contacts;

forming a plurality of polymer filled trenches on the first side between the dice having a depth less than the thickness;

forming a plurality of conductive vias in the dice in electrical communication with the die contacts;

thinning the substrate from the second side to expose the polymer filled trenches;

forming a plurality of grooves through the polymer filled trenches to singulate the dice; and

forming a plurality of terminal contacts on the dice in electrical communication with the die contacts.

77. The method of claim 76 further comprising etching the substrate following the thinning step to expose portions of the conductive vias to form the terminal contacts.

78. The method of claim 76 further comprising etching the substrate following the thinning step to expose tip portions of the conductive vias forming a plurality of terminal contacts on the die in electrical communication with the tip portions and forming the terminal contacts on the tip portions.

79. The method of claim 76 wherein the forming the conductive vias step comprising laser machining openings in the substrate, and at least partially filling the openings with a conductive material.

80. The method of claim 76 wherein the forming the conductive vias step comprises implanting a dopant on portions of the substrate and forming the conductive vias on the portions.

81. The method of claim 76 further comprising forming a first polymer layer on the first side, and a plurality of first contact bumps in the first polymer layer in electrical communication with the conductive vias.

82. The method of claim 76 further comprising forming a polymer layer on the second side, and a plurality of contact bumps in the polymer layer in electrical communication with the conductive vias, and then forming the terminal contacts on the contact bumps.

83. The method of claim 76 wherein the thinning the substrate step is performed by planarizing the substrate.

84. The method of claim 76 wherein the thinning the substrate step is performed by planarizing and then etching the substrate.

85. The method of claim 76 wherein the thinning the substrate step is performed by etching the substrate.

86. The method of claim 76 wherein the forming the grooves step is performed by sawing through the polymer filled trenches.

87. The method of claim 76 wherein the forming the grooves step is performed by etching through the polymer filled trenches.

88. The method of claim 76 wherein the forming the polymer filled trenches is performed by scribing the substrate with trenches and then filling the trenches with a polymer material.

89. The method of claim 76 wherein the forming the polymer filled trenches is performed by etching the substrate with trenches and then filling the trenches with a polymer material.

90. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side, a second side and a thickness, the dice comprising a plurality of die contacts;

forming a plurality of conductive vias in the dice in electrical communication with the die contacts; and

etching the substrate to expose portions of the conductive vias.

91. The method of claim 90 further comprising forming polymer filled trenches in the substrate then thinning the substrate from the second side prior to the etching step to expose the polymer filled trenches;

forming a plurality of grooves through the polymer filled trenches to singulate the dice; and

forming a plurality of terminal contacts on the dice in electrical communication with the die contacts.

92. The method of claim 90 wherein the exposed portions of the conductive vias comprise pins.

93. The method of claim 90 wherein the exposed portions of the conductive vias comprise pins in a pin grid array or a micro pin grid array.

94. The method of claim 90 further comprising forming a plurality of conductors on the second side in electrical communication with the exposed portions and a plurality of terminal contacts on the second side in electrical communication with the conductors.

95. The method of claim 94 wherein the terminal contacts comprise balls or bumps in a ball grid array.

96. The method of claim 94 wherein following the etching step the substrate has a second thickness of from 10 $\mu$m to 250$\mu$m.

97. A method for fabricating semiconductor components comprising:

providing a semiconductor substrate comprising a plurality of semiconductor dice having a plurality of die contacts, the substrate having a first side, a second side and a thickness;

forming a plurality of trenches on the first side along peripheral edges of the dice, each trench having a depth less than the thickness;

forming a plurality of contact bumps on the die contacts;

forming a plurality of conductive vias in the substrate in electrical communication with the contact bumps;

forming a first polymer layer on the contact bumps and in the trenches to form polymer filled trenches;

thinning the substrate from the second side to expose the polymer filled trenches; and

singulating the dice through the trenches such that each component includes a semiconductor die covered on at least five sides by a portion of the first polymer layer, and portions of the polymer filled trenches.

98. The method of claim 97 further comprising forming a second polymer layer on the second side, and forming a plurality of terminal contacts on the second polymer layer in electrical communication with the conductive vias.

99. The method of claim 97 further comprising etching the substrate following the thinning step such that the substrate is recessed with respect to the portions of the polymer filled trenches.

100. The method of claim 97 further comprising etching the substrate following the thinning step to form the

conductive vias as pins in a pin grid array or micro pin grid array.

101. The method of claim 97 further comprising etching or grinding the portions of the polymer filled trenches such that the portions are recessed with respect to the substrate.

102. The method of claim 97 further comprising forming a plurality of second contact bumps in the second polymer layer in electrical communication with the conductive vias and then forming the terminal contacts on the second contact bumps.

103. The method of claim 97 wherein the conductive vias comprise openings in the substrate, insulating layers on the openings and a conductive material in the openings.

104. The method of claim 97 wherein the conductive vias comprise portions of the substrate implanted with a dopant.

105. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a semiconductor substrate having a circuit side and a back side;

forming a plurality of trenches along peripheral edges of the dice part way through the substrate;

depositing a polymer material in the trenches;

forming a plurality of contact bumps on the dice;

forming a first polymer layer on the circuit side and the contact bumps;

forming a plurality of conductive vias in the dice in electrical communication with the contact bumps;

thinning the substrate from the back side to contact the polymer material in the trenches and to thin the back side;

forming a plurality of terminal contacts on the back side or on the circuit side in electrical communication with the conductive vias; and

singulating the dice by forming grooves through the trenches and the polymer material.

106. The method of claim 105 further comprising forming a second polymer layer on the back side and forming a plurality of second conductive vias in the second polymer layer in electrical communication with the conductive vias.

107. The method of claim 105 further comprising forming a plurality of second contact bumps on the back side following the thinning step in electrical communication with the conductive vias, and forming the terminal contacts on the contact bumps.

108. The method of claim 105 wherein the forming the conductive vias step comprises laser machining openings and at least partially filling the openings with a conductive material.

109. The method of claim 105 wherein the forming the conductive vias step comprises implanting a dopant into a selected portion of the substrate.

110. The method of claim 105 wherein the thinning the substrate step comprises mechanically planarizing the substrate.

111. The method of claim 105 wherein the contact bumps and the first polymer layer have a planarized surface.

112. The method of claim 105 wherein the thinning the substrate step comprises mechanically planarizing then etching the substrate.

113. The method of claim 105 wherein the thinning the substrate step comprises etching the substrate.

114. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side, a second side, and a plurality of die contacts on the first side;

forming a polymer layer on the first side having a plurality of first slots in a criss cross pattern between the dice;

forming an etch mask on the second side having a plurality of second slots aligned with the first slots;

forming a plurality of terminal contacts on the polymer layer in electrical communication with the die contacts; and

etching the substrate from the first side and the second side to singulate the dice.

115. The method of claim 114 further comprising following the etching step, forming a sealing layer on the second side and on edges of the dice.

116. The method of claim 114 wherein the sealing layer comprises parylene.

117. The method of claim 114 further comprising forming contact bumps on the die contacts, forming the polymer layer on the die contacts, and planarizing the contact bumps and the patterned polymer layer.

118. The method of claim 114 wherein the etching step is performed using KOH in a first etch step, and TMAH in a second step.

119. The method of claim 114 wherein the forming the polymer layer step comprises depositing a curable polymer through a stencil.

120. The method of claim 114 wherein the forming the polymer layer step comprises depositing and etching a polymer material.

121. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side, a second side, and a plurality of die contacts on the first side;

forming a plurality of contact bumps on the die contacts;

forming a polymer layer on the first side having a plurality of first slots in a criss cross pattern in which each die is enclosed by four slots;

planarizing the polymer layer and the contact bumps to a same surface;

forming an etch mask on the second side having a plurality of second slots aligned with the first slots;

forming a plurality of terminal contacts on the contact bumps;

etching the substrate from the first side and the second side to define edges of the dice; and

applying a coating to the edges and to the second side.

122. The method of claim 121 further comprising attaching a tape to the first side, and performing the etching step and the applying step with the tape covering the polymer layer and the contact bumps.

123. The method of claim 121 wherein the coating is configured to hermetically seal the second side and the edges.

124. The method of claim 121 wherein the terminal contacts comprise conductive bumps or balls.

125. The method of claim 121 wherein the forming the contact bumps step comprises attaching or depositing a solder material to the die contacts.

126. The method of claim 121 wherein the etching step is performed by submerging the substrate in a solution of KOH.

127. The method of claim 121 wherein the etching step is performed by submerging the substrate in a solution of TMAH.

128. The method of claim 121 wherein the substrate comprises a semiconductor wafer having streets separating the dice, and the first slots align with the streets.

129. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side, a second side, and a plurality of die contacts on the first side;

forming a plurality of contact bumps on the die contacts;

forming a polymer layer on the first side;

planarizing the polymer layer and the contact bumps to a same surface;

thinning the substrate from the second side;

forming a plurality of terminal contacts on the contact bumps; and

singulating the dice from the substrate.

130. The method of claim 129 further comprising following the thinning step applying a polymer tape to the second side.

132. The method of claim 130 wherein the polymer tape comprises a wafer level underfill material.

133. The method of claim 130 further comprising laser marking the polymer tape.

134. The method of claim 130 wherein the polymer tape is opaque to a radiation used for marking the polymer tape.

135. The method of claim 130 further comprising following the thinning step, attaching a heat sink to the second side.

136. The method of claim 130 wherein the forming the polymer layer step comprises forming a dam on the first side, depositing a curable material within the dam, and then curing the curable material.

137. The method of claim 129 further comprising testing the dice on the substrate prior to the singulating step.

138. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side, a second side, and a plurality of die contacts on the first side;

forming a polymer layer on the first side;

thinning the substrate from the second side;

singulating the dice from the substrate to form each component with a first side encapsulated by the polymer layer and a thinned second side; and

attaching a heat sink to the thinned second side.

139. The method of claim 138 further comprising forming a plurality of terminal contacts on the polymer layer in electrical communication with the die contacts.

140. The method of claim 138 further comprising forming a plurality of contact bumps on the die contacts encapsulated by the polymer layer.

141. The method of claim 138 wherein the singulating step is performed by sawing, laser cutting or liquid jet cutting the substrate.

142. The method of claim 138 wherein the attaching the heat sink step is performed using a thermally conductive adhesive.

143. A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side and a second side;

forming a plurality of trenches on the first side in a criss cross pattern between the dice;

forming a plurality of dams in the trenches comprising a first polymer material;

forming a plurality of polymer layers on the first side within the dams comprising a second polymer material;

thinning the substrate from the second side to expose the trenches; and

forming a plurality of grooves through the polymer dams to singulate the dice.

144. The method of claim 143 wherein the first polymer material comprises a photoimageable material.

145. The method of claim 143 wherein the first polymer material comprises a 3-D imageable material.

146. The method of claim 143 wherein the second polymer material comprises a silicone, a polyimide or an epoxy.

147. The method of claim 143 further comprising forming contact bumps on the dice within the polymer layers and forming terminal contacts on the contact bumps.

148. A method for fabricating semiconductor components comprising:

providing a semiconductor substrate comprising a plurality of semiconductor dice and having a first side, a second side and a thickness;

forming a plurality of trenches on the first side in a criss-cross pattern along peripheral edges of the dice, each trench having a depth less than the thickness;

depositing an imageable polymer material on the first side and in the trenches;

exposing and developing the imageable polymer material to form polymer dams in the trenches surrounding the dice;

depositing a second polymer material on the dice within the polymer dams;

thinning the substrate from the second side to expose the trenches; and

singulating the dice through the polymer dams such that each component includes a semiconductor die having a surface covered by a portion of the second polymer material and edges covered by portions of the first polymer material.

149. The method of claim 148 wherein the imageable polymer material comprises a photoimageable resist.

150. The method of claim 148 wherein the imageable polymer material comprises a 3-D imageable material.

151. The method of claim 148 wherein the second polymer material has selected electrical characteristics.

152. The method of claim 148 further comprising providing the dice with a plurality of die contacts, forming contact bumps on the die contacts embedded in the second polymer material, and forming terminal contacts on the contact bumps.

153. A semiconductor component comprising:

a thinned semiconductor die having a circuit side, a thinned back side and a plurality of peripheral edges;

a first polymer layer covering the circuit side and the edges; and

a second polymer layer covering the back side.

154. The semiconductor component of claim 153 further comprising a plurality of die contacts on the die, and a plurality of contact bumps on the die contacts embedded in the first polymer layer.

155. The semiconductor component of claim 154 further comprising a plurality of terminal contacts on the contact bumps.

156. The semiconductor component of claim 154 wherein the terminal contacts comprise bumps or balls in a grid array, or planar pads configured as an edge connector.

157. The semiconductor component of claim 154 wherein the second polymer layer is opaque to radiation at a selected wavelength.

158. The semiconductor component of claim 154 wherein the second polymer layer comprises a wafer level underfill tape.

159. The semiconductor component of claim 154 wherein the second polymer layer comprises parylene.

160. The semiconductor component of claim 154 wherein the second polymer layer comprises a photoresist.

161. The semiconductor component of claim 154 wherein the second polymer layer comprises a tape.

162. The semiconductor component of claim 154 wherein the second polymer layer comprises a stereographic imageable resist.

163. The method of claim 154 further comprising etching the substrate following the thinning step such that the substrate is recessed with respect to the portions of the polymer filled trenches.

164. The method of claim 163 wherein a thickness of the substrate following the etching step is about 10 μm to 250 μm.

165. The semiconductor component of claim 154 further comprising a polymer tape attached to the thinned back side which is opaque to radiation at a selected wavelength, and a laser marking on the polymer tape.

166. The semiconductor component of claim 154 further comprising a conductive via in the thinned substrate.

167. The semiconductor component of claim 166 wherein the conductive via comprises a conductive member exposed with respect to the substrate to provide a pin terminal contact.

168. The semiconductor component of claim 166 wherein the conductive via comprises a conductive member, a conductor on the back side and a terminal contact on the back side in electrical communication with the conductivity region.

169. The semiconductor component of claim 166 wherein the conductive via comprises a reverse bias junction.

170. A semiconductor component comprising:

a thinned semiconductor die having a circuit side, a back side, four peripheral edges, and a plurality of die contacts;

a plurality of contact bumps on the die contacts;

a first polymer layer covering the circuit side, the contact bumps and the peripheral edges;

a second polymer layer covering the back side; and

a plurality of terminal contacts on the contact bumps.

171. The semiconductor component of claim 170 wherein the contact bumps and the first polymer layer are planarized to a same surface.

172. The semiconductor component of claim 170 wherein the contact bumps comprise metal bumps.

173. The semiconductor component of claim 170 wherein the terminal contacts comprise conductive bumps or balls.

174. The semiconductor component of claim 170 wherein the first polymer layer has a planarized first surface.

175. The semiconductor component of claim 170 wherein the second polymer layer has a planarized second surface.

176. The semiconductor component of claim 170 further comprising a plurality of conductive vias in electrical communication with the die contacts and with the terminal contacts.

177. The semiconductor component of claim 176 further comprising a plurality of second die contacts on the second polymer layer in electrical communication with the conductive vias.

178. The semiconductor component of claim 170 wherein the second polymer layer comprises a photopolymer.

179. The semiconductor component of claim 170 wherein the second polymer layer comprises a wafer level underfill.

180. A semiconductor component comprising:

a thinned semiconductor die having a circuit side, a back side and four peripheral edges;

a circuit side polymer layer covering the circuit side;

a plurality of edge polymer layers covering the four peripheral edges, the edge polymer layers and the circuit side polymer layer comprising a continuous layer of material, the edge polymer layers comprising portions of polymer filled trenches; and

a back side polymer layer covering the back side.

181. The semiconductor component of claim 180 further comprising a plurality of die contacts on the die, and a plurality of contact bumps on the die contacts embedded in the circuit side polymer layer.

182. The semiconductor component of claim 180 further comprising a plurality of die contacts on the die, and a plurality of planarized contact bumps on the die contacts embedded in the circuit side polymer layer and planarized to a surface thereof.

183. The semiconductor component of claim 180 further comprising a plurality of terminal contacts on the contact bumps.

184. The semiconductor component of claim 180 further comprising a plurality of conductive vias through the die

185. The semiconductor component of claim 180 further comprising a plurality of conductive vias through the die including exposed portions configured as pins.

186. The semiconductor component of claim 180 further comprising a plurality of conductive vias through the die including tip portions, a plurality of conductors on the back side in electrical communication with the conductors, and a plurality of terminal contacts on the back side in electrical communication with the tip portions.

187. The semiconductor component of claim 180 wherein the back side polymer layer is opaque to radiation at a selected wave length.

188. The semiconductor component of claim 180 wherein the back side polymer layer comprises a wafer level underfill.

189. A semiconductor component comprising:

a semiconductor wafer having a circuit side and a back side, the wafer comprising a thinned substrate and a plurality of semiconductor dice on the thinned substrate separated by streets;

a plurality of polymer filled trenches in the thinned substrate in the streets;

a planarized circuit side polymer layer on the circuit side; and

a planarized back side polymer layer in the back side.

190. The semiconductor component of claim 189 further comprising a plurality of die contacts on the dice, and a plurality of contact bumps on the die contacts embedded in the planarized circuit side polymer layer.

191. The semiconductor component of claim 190 further comprising a plurality of terminal contacts on the contact bumps.

192. The semiconductor component of claim 191 further comprising a plurality of conductive vias in the substrate in electrical communication with the die contacts and with the terminal contacts.

193. The semiconductor component of claim 191 wherein the terminal contacts comprise bumps or balls in a grid array.

194. The semiconductor component of claim 191 wherein the terminal contacts are configured as an edge connector.

195. The semiconductor component of claim 191 further comprising a plurality of second terminal contacts on planarized back side polymer layer in electrical communication with the conductive vias.

196. A semiconductor component comprising:

a thinned semiconductor die having a circuit side, a back side, four peripheral edges, and a plurality of die contacts on the circuit side;

a first polymer layer covering the circuit side and the peripheral edges;

a plurality of conductive vias in the die in electrical communication with the die contacts;

a second polymer layer covering the back side;

and a plurality of terminal contacts in electrical communication with the conductive vias and the die contacts.

197. The semiconductor component of claim 196 wherein the terminal contacts are on the circuit side.

198. The semiconductor component of claim 196 wherein the terminal contacts are on the back side.

199. The semiconductor component of claim 196 wherein the terminal contacts are on both the circuit side and the back side.

200. The semiconductor component of claim 196 wherein the terminal contacts are offset from the conductive vias.

201. The semiconductor component of claim 196 wherein each conductive via comprise a reverse bias junction.

202. The semiconductor component of claim 196 wherein the terminal contacts are configured as an edge connector.

203. The semiconductor component of claim 196 wherein the terminal contacts are bonded to contact bumps on the die contacts.

204. The semiconductor component of claim 196 wherein the terminal contacts are bonded to planarized contact bumps on the die contacts planarized to a surface of the first polymer layer.

205. The semiconductor component of claim 196 wherein the conductive vias comprise openings in the die, insulating layers on the openings, and a conductive material in the openings.

206. The semiconductor component of claim 196 wherein the conductive vias comprise portions of the die implanted with a dopant.

207. The semiconductor component of claim 196 wherein the terminal contacts comprise portions of the conductive vias configured as pin contacts.

208. The semiconductor component of claim 196 wherein the terminal contacts comprise balls or bumps in an area array.

209. A semiconductor component comprising:

a thinned semiconductor die having a circuit side and a thinned back side;

a polymer layer covering the circuit side; and

a heat sink attached to the thinned back side.

210. The semiconductor component of claim 209 further comprising a thermally conductive adhesive attaching the heat sink to the thinned back side.

211. The semiconductor component of claim 209 wherein the die comprise a plurality of edges and the polymer layer covers the edges.

212. The semiconductor component of claim 209 wherein the die comprises a plurality of die contacts on the circuit side, contact bumps on the die contact and terminal contacts on the contact bumps.

213. The semiconductor component of claim 209 wherein the die comprises a plurality of die contacts on the circuit

side, planarized contact bumps on the die contact and terminal contacts on the planarized contact bumps.

214. A semiconductor component comprising:

a thinned semiconductor die having a circuit side and a thinned back side;

a polymer layer covering the circuit side;

a polymer tape attached to the thinned back side; and

a marking in the polymer tape.

215. The semiconductor component of claim 214 wherein the marking comprises a laser marking and the polymer tape is opaque to radiation of a selected wave length.

216. The semiconductor component of claim 214 wherein the die comprise a plurality of edges and the polymer layer covers the edges.

217. The semiconductor component of claim 214 wherein the die comprises a plurality of die contacts on the circuit side, contact bumps on the die contacts, and terminal contacts on the contact bumps.

218. The semiconductor component of claim 214 wherein the die comprises a plurality of die contacts on the circuit side, planarized contact bumps on the die contacts, and terminal contacts on the planarized contact bumps.

219. The semiconductor component of claim 214 wherein the polymer tape comprises a wafer level underfill.

220. A semiconductor component comprising:

a semiconductor die having a circuit side, a back side, four peripheral edges, and an array of die contacts on the circuit side;

a polymer layer covering the circuit side;

a protective coating covering the edges and the back side; and

a plurality of terminal contacts on the die contacts.

221. The semiconductor component of claim 220 further comprising a plurality of contact bumps on the die contacts.

222. The semiconductor component of claim 220 further comprising a plurality of planarized contact bumps on the die contacts planarized to a surface of the polymer layer.

223. The semiconductor component of claim 220 wherein the protective coating comprises parylene.

224. The semiconductor component of claim 220 wherein the terminal contacts comprise bumps or balls in a grid array.

225. The semiconductor component of claim 220 wherein the terminal contacts are configured as an edge connector.

226. The semiconductor component of claim 220 wherein the peripheral edges comprise etched surfaces.

227. A semiconductor component comprising:

a thinned semiconductor die having a circuit side, a back side, four peripheral edges, and a plurality of die contacts;

a first polymer layer covering the circuit side comprising a first polymer material; and

a plurality of second polymer layers covering the peripheral edges comprising a second polymer material.

228. The semiconductor component of claim 227 further comprising a plurality of contact bumps on the die contacts embedded in the first polymer layers and a plurality of terminal contacts on the contact bumps.

229. The semiconductor component of claim 228 wherein the contact bumps and the first polymer layer are planarized to a same surface.

230. The semiconductor component of claim 228 wherein the contact bumps comprise conductive bumps or balls.

231. The semiconductor component of claim 228 wherein the second polymer layers comprise a photoimageable resist.

232. The semiconductor component of claim 228 wherein the second polymer layer comprise a stereo lithographic imageable material.

233. A semiconductor component comprising:

a thinned semiconductor die having a circuit side, a back side, and a plurality of die contacts on the circuit side;

a plurality of conductive vias in the die in electrical communication with the die contacts;

and a plurality of terminal contacts in electrical communication with the conductive vias and the die contacts comprising pin contacts.

234. The semiconductor component of claim 233 wherein the pin contacts comprise conductive portions of the conductive vias.

235. The semiconductor component of claim 233 wherein the pin contacts comprise a pin grid array.

236. The semiconductor component of claim 233 wherein each conductive via comprises a reverse junction bias.

237. The semiconductor component of claim 233 further comprising a second polymer layer covering the back side.

238. The semiconductor component of claim 233 wherein the thinned die has a thickness of from about 10 μm to 250 μm.

239. The semiconductor component of claim 233 further comprising a first polymer layer covering at least the circuit side.

240. The semiconductor component of claim 239 wherein the first polymer layer covers edges of the die.

241. The semiconductor component of claim 239 further comprising a second polymer layer covering the back side.

242. A semiconductor component comprising:

a thinned semiconductor die having a circuit side, a back side, and a plurality of die contacts on the circuit side;

a plurality of conductive vias in the die in electrical communication with the die contacts;

and a plurality of terminal contacts in electrical communication with the conductive vias and the die contacts comprising tip portions projecting from the thinned semiconductor die;

a plurality of conductors in electrical communication with the tip portions; and

a plurality of terminal contacts in electrical communication with the conductors.

243. The semiconductor component of claim 242 wherein the tip portions comprise a conductive material.

244. The semiconductor component of claim 242 wherein the terminal contacts comprise ball or bumps in a grid array.

245. The semiconductor component of claim 242 wherein the conductive vias comprise reverse bias junctions.

246. The semiconductor component of claim 242 further comprising a first polymer layer covering at least the circuit side.

247. The semiconductor component of claim 246 wherein the first polymer layer covers edges of the die.

248. The semiconductor component of claim 246 further comprising a second polymer layer covering the back side.

249. A system comprising:

a substrate; and

a component on the substrate comprising:

a thinned semiconductor die having a circuit side, a back side and a plurality of peripheral edges;

a first polymer layer covering the circuit side and the edges;

a second polymer layer covering the back side; and

a plurality of terminal contacts on the first polymer layer in electrical communication with the die and bonded to the substrate.

250. The system of claim 249 further comprising a plastic body encapsulating the substrate and the component.

251. The system of claim 249 further comprising a plurality of planarized contact bumps on the die embedded in the first polymer layer.

252. The system of claim 249 wherein the substrate comprises a plurality of terminal leads in electrical communication with the terminal contacts.

253. The system of claim 249 wherein the substrate comprises an edge connector in electrical communication with the terminal contacts.

254. The system of claim 249 wherein the system comprises a system in a package.

255. The system of claim 249 wherein the substrate comprises a module substrate and the system comprises a multi chip module.

256. A system in a package comprising:

a substrate comprising a plurality of terminal leads;

a component mounted to the substrate, the component comprising:

a thinned semiconductor die having a circuit side, a back side, four peripheral edges, and an area array of die contacts;

a plurality of contact bumps on the die contacts;

a first polymer layer covering the circuit side, the contact bumps and the peripheral edges;

a second polymer layer covering the back side; and

a plurality of terminal contacts on the contact bumps in electrical communication with the terminal leads; and

a plastic body encapsulating the substrate and the component.

257. The system of claim 256 wherein the terminal contacts comprise bumps or balls and the component is flip chip mounted to the substrate.

258. The system of claim 256 wherein the terminal contacts comprise an edge connector and the component is edge connector mounted to the substrate.

259. A stacked semiconductor system comprising:

a first semiconductor component comprising:

a thinned semiconductor die having a circuit side, a back side, four peripheral edges, and an array of die contacts on the circuit side;

a plurality of contact bumps on the die contacts;

a first polymer layer covering the circuit side, the peripheral edges, and portions of the contact bumps;

a plurality of conductive vias in the die in electrical communication with the contact bumps;

a second polymer layer covering the back side; and

a plurality of terminal contacts on the back side in electrical communication with the conductive vias; and

a second semiconductor component substantially identical to the first semiconductor component comprising a plurality of second terminal contacts bonded to the contact bumps.

260. The stacked semiconductor system of claim 259 wherein the conductive vias comprise openings in the die, insulating layers on the openings, and a conductive material in the openings.

261. The stacked semiconductor system of claim 259 wherein the terminal contacts comprise balls or bumps in a grid array.